Abstract Of The Invention

The invention includes a process for manufacturing an integrated circuit, comprising providing a substrate comprising a dielectric layer over a conductive material, depositing a hardmask over the dielectric layer, applying a first photoresist over the hardmask and photodefining a trench, etching the hard mask and partially etching the dielectric to form a trench having a bottom, stripping the photoresist, applying a second photoresist and photodefining a slit across the trench, selectively etching the dielectric from the bottom of the trench down to the underlying conductive material. Both the hardmask and the second photoresist are used as a mask. Later, a connection to the underlying metal is formed and integrated circuits made thereby.